

PCI Express® M.2 Specification

Revision 4.0 Version 0.3

September 26, 2018



Note to Reviewers:

This specification includes only the high level directions and requirements for the PCI Express 4.0 M.2 specification as approved by the PCIe Mini workgroup. Please provide feedback on these items and any additional requirements that you believe should be covered in the 4.0 M.2 specification.

PCI Express M.2 Specification, Rev 4.0, Version 0.3

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1. Support signaling rates of 16 GT/s, 8 GT/s, 5 GT/s and 2.5 GT/s
2. Specification References list updated to reference the latest specifications:

Spec References

71 **1.3. Specification References**

72 This specification requires references to other specifications or documents that will form the basis

73 for some of the requirements stated herein.

74 ☐ *PCI Express Mini Card Electromechanical (CEM) Specification, Revision 2.0*

75 ☐ *PCI Express Card Electromechanical (CEM) Specification, Revision 3.0*

76 ☐ *Advanced Configuration and Power Interface (ACPI) Specification, Revision 2.0b*

77 ☐ *PCI Express Base Specification, Revision 3.1*

78 ☐ *SDIO3.0*

79 ☐ *SSIC – SuperSpeed USB Inter-Chip Supplement to the USB 3.0 Specification, Revision 1.0 as of*

80 *May 3, 2012*

81 ☐ *HSIC - High-Speed Inter-Chip USB Electrical Specification, Version 1.0 (September 23, 2007), plus*

82 *HSIC ECN Disconnect Supplement to High Speed Inter Chip Specification, Revision 0.94 (Sep 20, 2012)*

83 ☐ *USB2.0 - Universal Serial Bus Specification, Revision 2.0, plus ECN and Errata, July 14, 2011,*

84 *available from <http://www.usb.org>*

85 ☐ *USB3.1 - Universal Serial Bus Specification, Revision 3.1, plus ECN and Errata, available from*

86 *<http://www.usb.org>*

87 ☐ *DisplayPort Standard Specifications, version 1.2*

88 ☐ *ISO/IEC 7816-2 Specification*

89 ☐ *ISO/IEC 7816-3 Specification*

90 ☐ *Serial ATA Specification, available from www.sata-io.org*

91 ☐ *PC BUS Specifications, Version 2.1, January 2000*

92 ☐ *ELA-364 Electrical Connector/Socket Test Procedures including Environmental Classifications*

93 ☐ *ELA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors*

94 *and Sockets Used in Business Office Applications*

95 ☐ *M-PHY - MIPI Alliance Specification for M-PHY, Version 3.0*

96 ☐ *MIPI Alliance Specification for RF Front-End Control Interface (RFFESM), Version 2.0, September 25, 2014*

97 ☐ *JTAG Specification (IEEE 1149.1), available from <https://www.ieee.org>*

98 ☐ *System Management Bus (SMBus) Specification, Version 2.0, August 3, 2000, available from*

99 *<http://smbus.org/>*

100 ☐ *BT-SIG – Draft Improvement Proposal Document for Coexistence, v10r00, January 19, 2010*

Change to “PCI Express Card Electromechanical Specification, Revision 4.0, Version 0.7”

Change to “PCI Express Base Specification, Revision 4.0, Version 1.0”

Change to “USB 3.2 – Universal Serial Bus 3.2 Specification, Revision 1.0”

Change to Version 3.1, March 19, 2018

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3. Clocking

Following clocking architectures will be supported:

- Common Reference Clock
- Separate Reference Clock with Independent SSC (SRIS)
- Separate Reference Clock No SSC (SRNS)

4. No connector changes needed to support 16 GT/s on M.2 connectors. Standalone connector Signal Integrity requirements to be updated as follows:



Signal Integrity Guideline

Table 6-1. Signal Integrity Parameters and Test Procedures for M.2 Connectors



Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: <ul style="list-style-type: none"> The measured differential S-parameter shall be referenced to 85 Ω differential impedance. The test fixture shall meet the test fixture recommendations defined in Section 6.3.1. The test fixture effect shall be removed from the measured S-parameters. See Note 1. 	≥ -0.5 dB up to 4 GHz; $\geq [-0.25*f + 0.5$ dB for 4 GHz $< f < 8$ GHz] for example -1.5 dB at 8 GHz $\geq [-0.75*f + 4.5$ dB for 8 GHz $< f < 10$ GHz For example: -3.0 dB at 10 GHz
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: <ul style="list-style-type: none"> The measured differential S-parameter shall be referenced to 85 Ω differential impedance. The test fixture shall meet the test fixture recommendations defined in Section 6.3.1. The test fixture effect shall be removed from the measured S-parameters. See Note 1. 	≤ -15 dB up to 3.0 GHz; $\leq [5*f - 30$ dB for $3.0 < f < 4.4$ GHz]. For example: -10 dB at 4 GHz ≤ -8.0 dB from 4.4 to 10 GHz;



NEXT and FEXT

Intra-pair Skew (Soldered-down BGA)	Intra-pair skew must be achieved by design; measurement not required.	1 ps max
Intra-pair Skew (BGA mounted on the M.2 Add-in Card)	Intra-pair skew must be achieved by design; measurement not required.	2 ps max
Differential Near End Crosstalk (DDNEXT) and Differential Far End Crosstalk (DDFEXT)	<p>EIA 364-90</p> <p>The EIA standard must be used with the following considerations:</p> <ul style="list-style-type: none"> The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. This is a differential crosstalk between a victim differential signal pair and all adjacent differential signal pairs. The measured differential S-parameter shall be referenced to 85 Ω differential impedance. 	<p>≤ -32 dB up to 8 GHz and -20 dB from 8 GHz to 10 GHz;</p>

5. Add following IL budget requirements:



IL Budget

- Add Section 3.5 “Electrical Budgets”
- Add following text to this section:
- **3.5.1. Add-in Card Insertion Loss Limit for 16GT/s**

The insertion loss from the top of edge finger to the silicon pad for both Receiver and Transmitter interconnect must not exceed 6.5 dB at 8 GHz for SSDs. Other applications are not required to follow this IL limit but need to make sure that the total IL at 8GHz does not exceed 8dB.

This loss includes PCB routing, vias, AC Cap and silicon package

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6. Add Standalone Connector test guidelines in the Signal Integrity section.

- Elaborate on the Victim/Aggressor high speed signal pair arrangement to capture worse case cross-talk on the connector.

7. Update the test fixtures recommendations and golden finger Ground voiding guidelines to support 16 GT/s

8. Add Transmitter Equalization details

- Add Preset test requirements at 16 GT/s

9. Define Eye Diagrams at the Add-in Card Interface

- a. Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s
- b. Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s
- c. System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s
- d. System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

10. Define Adapter Transmitter Path Pulse Width Jitter (PWJ) limits at 16 GT/s

11. Define 16 GT/s Test channels and distribute with the specification.

- a. System board test channel (S-parameters)
- b. Add-in Card test channel (S-parameters)